PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: John Quernemoen

Serial No.: 09/515,158 Examiner: Dodds, Harold E.

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For: BUILD IN HEADROOM FOR AN NT SYSTEM SIZER

Docket No.: RA-5247 (1028.1126101)

DECLARATION UNDER RULE 1.131

Mail Stop Non-Fee Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

CERTIFICATE UNDER 37 C.F.R. 1.8: I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on this 13th day of November, 2003.

By: _____
Brian N. Tufte

Dear Sir:

I, John M. Quernemoen and Mark G. Hazzard, as the joint inventors of the claimed inventions of the above-identified application, declare as follows:

This Declaration is to establish completion of the inventions in this application in the United States, at a date prior to April 30, 1999, which is the effective filing date of the Yang et al. patent (U.S. Patent No. 6,542,845).

Facts and Documentary Evidence

All work on the inventions included in the above-identified application was completed in the United States.

The inventions included in this application were completed prior to April 30, 1999. As evidence of this, attached hereto as Exhibit 1 is a true and accurate copy of an e-mail from John M. Quernemoen to a number of employees within Unisys, with only the dates redacted. The date identified on the e-mail (which has been redacted in the attached copy) indicates that the email was sent prior to April 30, 1999.

The e-mail shown in Exhibit 1 shows that an updated version of the NT sizer program was completed and distributed to the recipients identified in the e-mail. The email also documents that two attachments were provided, including an NTSizer_280.exe file and an NT Sizer User Guide.exe file. The NTSizer_280.exe file contained a program that implemented the inventions claimed in the above-identified application. The NT Sizer User Guide.exe file contained the User Guide for the NTSizer_280.exe program. Because both of these files were attached to the e-mail of Exhibit 1, the NTSizer_280.exe program and the NT Sizer User Guide were completed prior to April 30, 1999.

Attached hereto as Exhibit 2 is a true and accurate copy of the NT Sizer User Guide, with only the dates redacted. Beginning at the last full paragraph of page A-21, the NT Sizer User Guide states:

> The maximum processor utilization is the processor utilization level that you do not wish to exceed with the specified workload on the proposed system. Specifying a maximum of 100% is not recommended, as response times degrade as the processor utilization approaches 100%, and it also provides no room for growth. Specifying a value too low will provide configuration requirements that far exceed the input requirements. If you do not have a processor utilization number in mind, use 80-85% as this will provide a reasonable estimate with a safety margin. Since this type of sizing is based on a TPC-C workload, you must also specify the tpmC requirement. If you do not know what tpmC value to use, start with a baseline system and increase or decrease the tpmC value accordingly.

Once the baseline and target system characteristics have been selected, click the **Calculate** button. Results of the calculations are shown in the lower right quadrant of the dialog.

For example, in the dialog above, the Unisys QS/2 server with the Xeon 400 Mhz processor is being compared to the Acer 4 way system with the 200 Mhz processor. The tpmC requirement was input as 14000 on the QS/2 server with a requirement that the processor utilization not exceed 80%. This results in a configuration requiring 4 processors that will operate at 77% utilization on the average. Further, this system provides 26% more throughput than the baseline. Also shown are the estimated processor and memory requirements of 4096 MB and 978 GB, respectively.

As can be seen, the NT Sizer User Guide documents that the NTSizer_280.exe program implemented a method for sizing the hardware resources for a yet-to-be built database management system. The NT Sizer User Guide also documents that the method included the step of providing one or more desired hardware utilization limits for the yet-to-be built database management system. In the example described beginning on page A-21 of the NT Sizer User Guide, a maximum processor utilization limit is provided. In the example described at the last paragraph of page A-23 of the NT Sizer User Guide, a maximum network interface card utilization is provided. The NT Sizer User Guide also documents that the method included the step of obtaining one or more throughput workload requirements for the yet-to-be built database management system. In the example described beginning on page A-21 of the NT Sizer User Guide, a TPC-C workload requirement is obtained. The NT Sizer User Guide also documents that the method included the step of determining the hardware resources needed for the yet-to-be built database management system to satisfy the one or more throughput workload requirements while remaining within the desired hardware utilization. In the example described beginning on page A-21 of the NT Sizer User Guide, a number of processors are determined to meet the throughput workload requirement while remaining within the desired hardware utilization. Also,

in section 3.3, and beginning on page A-13, the NT Sizer User Guide documents that selected database requirements may be obtained including an expected database size.

The GUI shown on the top of page A-21 of the NT Sizer User Guide documents that the user can enter changes to the hardware utilization limits and the workload requirement, and by clicking on the calculate button, re-determining the hardware resources needed to remain within the desired hardware utilization limits.

In view of the foregoing, and in view of the above submitted evidence, the inventions included in this application were completed prior to April 30, 1999.

All statements made herein are of my own knowledge and are true and all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Date: 11/12/03

John M. Quernemoen

Date: 11/12/03

Mark G. Hazzard